IN THE SPECIFICATION

Please replace the third paragraph of page 8 with the following:

Sub B1

A1

Refer now to Fig. 5, schematically depicting the method of the present invention. A Flash EPROM cell 52 is to be erased. The cathode of a protective diode 38 is connected to a charge pump circuitry 36. The anode of the protective diode 38 is connected to one (or more) diode-connected NMOS transistor(s) 40, for example. A diode-connected NMOS transistor is one where the drain and gate are connected. When conducting, the voltage drop across each diode-connected NMOS transistor will be equal to the transistor threshold voltage (V_t).

Please replace the first full paragraph of page 9 with the following:

Sub B2

A2

The function of the margin erase circuit of the present invention is now described. During normal operation of the Flash EPROM cell 52, the bypass switch 50 is opened. The voltage, V_E, regulated by this regulator will be the normal erase voltage (V_{NE}), which is the sum of the voltage drops across transistors 46a-46n and 40 and the breakdown voltage (V_{bd}) of the protective diode 38. Since the voltage drop across each transistor 46a-46n and 40 is equal to V_t (threshold voltage of NMOS transistor), the normal erase voltage observed at the cathode of the protective diode 38 is given by:

$$V_{NE} = V_{bd} + V_t + n*V_t .$$